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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/003,673	11/02/2001	Norbert Felber	PHCH000024	5324

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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2133	5

DATE MAILED: 04/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/003,673	FELBER ET AL.	
	Examiner	Art Unit	
	James C Kerveros	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☒ Claim(s) *1-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement filed January 24, 2003 fails to comply with 37 CFR 1.98(a)(1), which requires a list of all patents, publications, or other information submitted for consideration by the Office. The Applicant should include the applicable documents in an Information Disclosure Statement (PTO-1449).

It has been placed in the application file, but the information referred to therein has not been considered.

Specification

The disclosure is objected to because it fails to comply with the preferred layout.

The following headings are missing in the specification:

(a) TITLE OF THE INVENTION.

(b) CROSS-REFERENCE TO RELATED APPLICATIONS.

(e) BACKGROUND OF THE INVENTION.

(1) Field of the Invention.
(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.

(f) BRIEF SUMMARY OF THE INVENTION.

(g) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).

(h) DETAILED DESCRIPTION OF THE INVENTION.

Appropriate correction is required by inserting each heading to a corresponding section.

Claim Objections

Claims 1-13 are objected to because of the following informalities:

The reference designations and the acronyms enclosed in the parenthesis should be deleted, because that which is included in the claims in a parenthesis is not given patentable weight. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 4 and 8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 4, on line 5, recites: " whereby ...." Such recitation is non-functional language, and as a result, is not given patentable weight. It has been held that functional "whereby" statement does not define any structure and accordingly cannot serve to distinguish in re Mason, 114 USPQ, 44 CCPA 937 (1957).

Claim 8 is, also, rejected because it depends upon a rejected claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the

applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-7 and 9-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Sengoku (US 6219808).

Regarding independent Claims 1 and 9, Sengoku discloses a method and apparatus for fault detect testing of semiconductor integrated circuits, comprising:

A circuit cell CMOS transistors (Qp11, Qp12, Qn11, Qn12) to be tested in the integrated circuit (G11), and separating the circuit cell into two independent cell networks (Qp11, Qp1 2 and Qn11, Qn12), FIG. 5B.

Obtaining a first response in a "stuck-at-1" fault test mode at the output of G1 (OUT1) for the first (Qp11, Qp12) of said two independent cell networks (Qp11, Qp12 and Qn11, Qn12), (column 5, lines 47-54).

Obtaining a second response in a "stuck-at-0" fault test mode at output of G1 (OUT1) for the second of (Qn11, Qn12) of the two independent cell networks (Qp11, Qp12 and Qn11, Qn12), (column 5, lines 55-62) and processing the first response sequence and the second response sequence in order to detect a defect in said circuit cell.

Regarding Claims 2 and 3, Sengoku discloses comparing the first response with the second response to detect an inconsistency and comparing the first response and the second response with expected responses to detect an inconsistency, describing,

"the output pattern is compared with an expected pattern. Thus, a determination of whether or not the device is normal or abnormal is made based on whether or not the output pattern coincides with the expected pattern" (column 1, lines 17-20).

Regarding Claims 4 and 10, Sengoku discloses a power supply VDD for powering up the circuit cell CMOS (Qp11, Qp12, Qn11, Qn12) and selecting p- (Qp11, Qp12) and n-channel (Qn11, Qn12) transistor networks in the circuit cell.

Putting the circuit cell (CMOS) a "stuck-at-1" fault and "stuck-at-0" fault test mode, where the p- and n-channel are stimulated by a sequence of test vectors (logic levels) at the input IN11 and IN12, such as logic levels "low" or "high" for obtaining responses at the output OUT1 from the p- (Qp11, Qp12) and n- channel (Qn11, Qn12). If input IN11 and IN1 2 is low, then the output OUT1 is "high". If both IN1 1 and IN1 2 are high, then the output OUT1 is low, (column 3, line 27-30) describing a logic operation for a two input NAND GATE, and determining a defect detected based upon an inconsistency between the actual responses at the output OUT.sub.1, (column 1, lines 17-20).

Regarding Claims 5 and 11, Sengoku discloses means (Qp13, Qp14 and Q13, Qn14) control transistors used to electrically separate the circuit cell into first (Qp11, Qp1 2) and second (Qn11, Qn12) independent cell, FIG. 5B.

Regarding Claims 6, 12, Sengoku discloses load means (resistor F1) having a small resistance connected between the G1 output and the power supply line VDD, while in the test mode, FIG. 3A.

Regarding Claim 7, Sengoku discloses measuring the current drain Idd of the circuit cell CMOS device, and determining if a defect is detected in the load (F1) based upon the amount of the current drain Idd at an quiescent state, such that a fault is detected by detecting an abnormal quiescent VDD supply current Iddq, i.e., a penetration current flowing within the CMOS device (col. 4, lines 65-67). Also, in a "stuck-at-1" fault, FIG. 7A, a current flows from the power supply VDD via the "stuck-at-1" fault (resistor F1) to GND, which can be detected by a current detector (not shown) connected to the power supply line VDD or GND, (col. 6, lines 54-61).

Regarding Claim 13, Sengoku discloses connection circuitry (PON, POFF) and (NOFF, NON) connecting electrical signals, such as control logic levels coupled to the control circuitry (Qp13, Qp14 and Q13, Qn14) for the purpose of testing other circuits under test by selectively turning the control circuitry on / off, FIG. 5B.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sengoku (US 6219808).

Regarding Claim 8, Sengoku does not disclose suppressing leakage currents in the circuit cell by turning off the control means while the circuit cell is in standby mode. However, Sengoku substantially discloses control transistors (Qp13, Qp14 and Q13, Qn14) for controlling the circuit cell, so that, for example, by turning transistors (Qp13, Qp14) "off" in response to the input control logic levels at PON and POFF, the current Idd from the power supply VDD does not flow through the cell CMOS transistors (Qp11, Qp12, Qn11, Qn12), thus causing a reduction in the leakage currents through the circuit cell. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to turn the control transistors "off" in the device of Sengoku, thus reducing the flow of current through the cell CMOS, as to avoid unnecessary heat dissipation during the standby mode.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James C Kerveros whose telephone number is (703) 305-1081. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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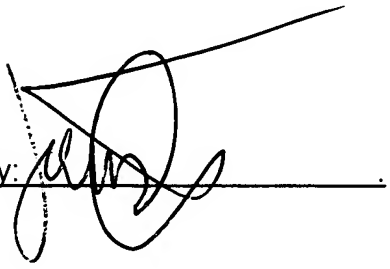
By: 

Date: 19 March 2004
Office Action: Non-Final Rejection

James C Kerveros
Examiner
Art Unit 2133